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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,406	01/26/2004	Darrell Rinerson	UNTYP030	2199

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,406	RINERSON ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments with respect to amended claims 1-45, filed 05/16/2005, have been considered but they are moot in view of new ground(s) of rejection.

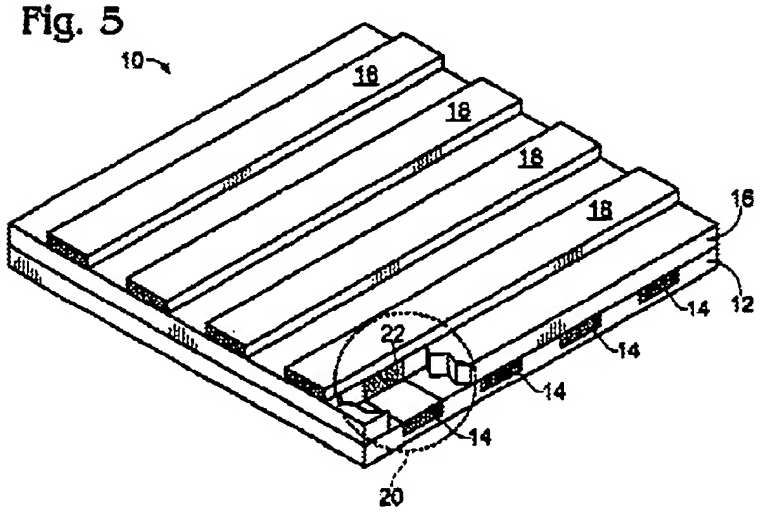
Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

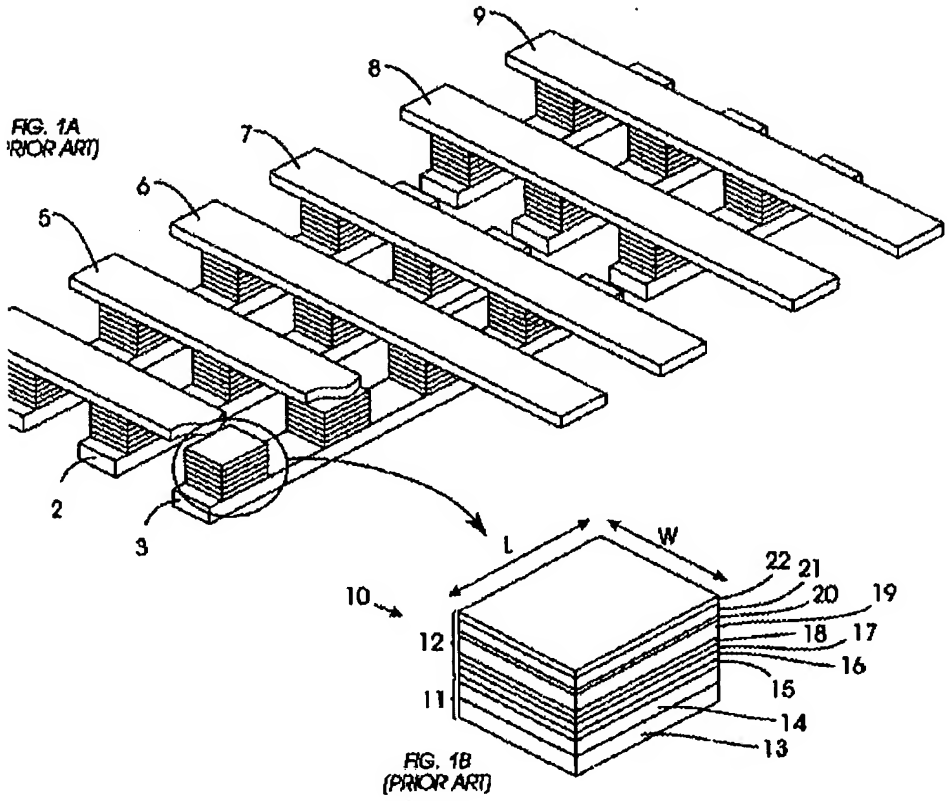
A. State of the art

a. Memory cells are arranged into arrays: at the time the invention was made, resistive memory cells were normally arranged into an array together with x-direction lines and y-direction lines, and each of the memory cells was arranged at each of the intersection of the x-direction lines and the y-direction lines so as each individual cell could be utilized individually. One such cross-point memory array is disclosed by Hsu et al. U.S. Patent 6,693,821 (the '821 reference), cited in a previous office action. The '821 reference discloses in Fig. 5 a memory device 10 comprising memory cells arranged at each of the intersection of the x-direction lines 14 and the y-direction lines 18 so as each individual cell could be utilized individually.

Fig. 5



b. Memory device with a steering (non-linear selection) device: at the time the invention was made, a simple steering device, such as a diode – rather than a transistor - as a design selection, was fabricated in series with a memory cell so as to obtain a simple structure with only two terminals per cell. Such a system is disclosed by Monsma et al. U.S. Patent 6,331,944 ('the '944 reference, Figs. 1-2 and column 3, lines 3-28). The '944 reference discloses a memory device with a steering device 13/14 and simple electrode structures 15/16 and 22:



c. Memory device with elaborate bottom electrode structures: at the time the invention was made, bottom elaborate electrode structure including a diffusion barrier layer and

a seed and or seed/template layer was chosen, as a matter of simple design selection, so as, as the labels suggest, to provide a diffusion barrier preventing diffusion of undesirable materials onto underlying, previously formed layers and to provide a seed/template layer from which overlying, later formed layers are formed. Such a memory device is disclosed by Slaughter et al. U.S. Patent 6,544,801 (the '801 reference), cited in a previous office action. The '801 reference discloses a memory system including a memory cell 50 comprising a bottom electrode structure 54 having a metal layer 72, a diffusion barrier layer 74, a seed layer 76, and a template layer 78.

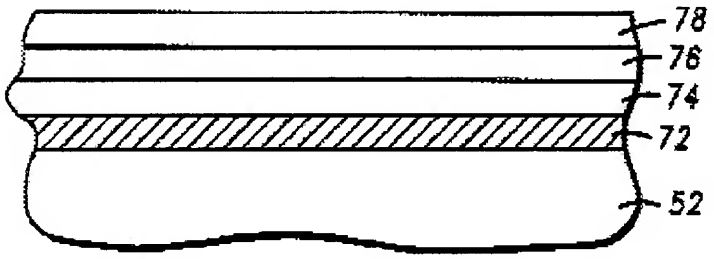


FIG. 7

d. Memory device with simple top electrode structures: at the time the invention was made, it was known to chose a low-processing-temperature material for the top electrode so as to minimize the diffusion of the top electrode material into the previously formed underlying memory layer. Such a memory device with a simple top electrode is disclosed by Gudesen et al. U.S. Patent Application Publication 20030179617, paragraph [0077].

2. **Claims 1-4,7-10,25 and 28** are rejected under 35 U.S.C. 103(a) as obvious over Hsu et al. U.S. Patent Application Publication 20040235247 (the '247 reference) in view of Hsu et al. U.S. Patent 6,693,821 (the '821 reference).

Referring to **claims 1, 3-4, 10, 25, and 28**, the '247 reference discloses a memory device, comprising:

a substrate (inherent) having a deposition face;

a multi-resistive state memory cell, wherein at least a portion of the memory cell is formed using high temperature processing at a first temperature (paragraph [0036], the crystalline portion), and each of the memory cells includes at least two EPVR (electrical pulse various resistance) conductive metal oxide layers that are not identical to each other (paragraphs [0009], [0024]-[0026], layers 404 and 406; specifically, the reference discloses: "EPVR first and second layers 404/406 are a material such as CMR, HTSC, or perovskite metal oxide materials", emphasis added, and "layer 404 having a polycrystalline structure EPVR.... second layer 406 is adjacent the first layer 404, having either a nano-crystalline or amorphous structure", emphasis added);

a bottom refractory metal layer (402) that has a melting point above the first temperature, parallel to the deposition face of the substrate, patterned into bottom conductive array lines; and

a top metal layer (408), parallel to the deposition face of the substrate, the memory cell capable of being programmed by application of voltages through the bottom refractory metal layer and the top metal layer.

However, the reference fails to disclose that the single memory cell is formed into an array of memory cells.

Nevertheless, as detailed above in paragraph A.a, at the time the invention was made, memory cells were normally arranged into an array so as to have a memory system with more memory capacity than a system of just a single cell, together with x-direction lines and y-direction lines, and each of the memory cells was arranged at each of the intersection of the x-direction lines and the y-direction lines so as each individual cell could be utilized individually.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's memory cell into an array of cells. One would have been motivated to make such a change because memory cells arranged into an array provides a memory system with more memory capacity than a system of just a single cell. A memory device such modified hereinafter is simply referred to as the '247/821 reference.

Referring to **claims 7-9** and again to **claim 25**, although not explicitly disclosed, the bottom refractory metal layer 402 of a material such as Ta, Pt, , Ag, Au, or Ir (paragraph [0025]) (cited as "conductive lines beneath the multi-resistive state element" in claim 25, as "the first metal layer" in claim 33, and as "a bottom plurality of layers" in claim 44) has a melting point of at least 700C, is stable at 600C, and is stable at the high temperature processing.

Referring to **claim 2**, the resistance of the '247 reference's programmable-erasable (paragraph [0007]) nonvolatile EPVR (electrical pulse various resistance) can be reversibly programmed to different values.

3. Claims 5-6, 26-27, 33-37, 39-40, and 44 are rejected under 35 U.S.C. 103(a) as obvious over Hsu et al. U.S. Patent Application Publication 20040235247 (the '247 reference) in view of

Hsu et al. U.S. Patent 6,693,821 (the '821 reference) and further in view of Gudesen et al. U.S. Patent Application Publication 20030179617 (the '617 reference).

Referring to **claims 5-6, 26, 33-37, 39, and 44**, the '247/821 reference discloses a memory device as claimed and as detailed above for claims 1 and 25 including the top refractory/noble metal layer 408 (otherwise known as the top electrode in the art, cited as "the second metal layer" in claim 33 and as "a top plurality of layers" in claim 44), but fails to teach that the top metal layer is not a refractory metal (in re claim 5), not stable at the high temperature, not stable at the minimum temperature required for fabrication (claim 33) (of the memory element), and not stable at the first temperature (claim 44) (to fabricate the memory element).

However, at the time the invention was made, Gudesen teaches choosing a low-processing-temperature material for the top electrode so as to minimize the diffusion of the top electrode material into the previously formed underlying memory layer.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the top electrode layer of the '247/821 reference such that it is a low-processing-temperature material. One would have been motivated to make such a change because Gudesen teaches choosing a low-processing-temperature material for the top electrode minimizing the diffusion of the top electrode material into the previously formed underlying memory layer. A memory device such modified hereinafter is simply referred to as the '247/821/617 reference, and a top electrode of such a device is of course of a low-processing-temperature material, such as aluminum or copper (in re claims 5-6 and 36-37) and not a refractory metal as is known, and consequently not stable at the minimum temperature required

for fabrication of the memory element and not stable at the first temperature to fabricate the memory element.

Referring to **claim 27**, the '247 reference's programmable-erasable (paragraph [0007]) nonvolatile multi-resistive state EPVR (electrical pulse various resistance) is rewritable.

Referring to **claim 40**, the '247 reference's (bottom) electrode includes gold ("Au", paragraph [0025]).

4. **Claims 11-23 and 29-33** are rejected under 35 U.S.C. 103(a) as obvious over Hsu et al. U.S. Patent Application Publication 20040235247 (the '247 reference) in view of Hsu et al. U.S. Patent 6,693,821 (the '821 reference) and further in view of Slaughter et al. U.S. Patent 6,544,801 (the '801 reference).

Referring to **claims 11, 23, and 29**, the '247/821 reference discloses a memory device as claimed and as detailed above for claims 1, 10, and 25 including the bottom electrode 402, but fails to teach that the bottom electrode further includes a barrier layer as claimed.

However, at the time the invention was made, Slaughter discloses a memory system including a memory cell 50 comprising a bottom electrode structure 54 having an electrode including a metal layer 72 and a diffusion barrier layer 74 so as to provide a diffusion barrier preventing diffusion of undesirable materials onto underlying, previously formed layers.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the electrode layer of the '247/821 reference such that it includes a barrier layer. One would have been motivated to make such a change because Slaughter teaches that a memory system including a memory cell comprising a bottom electrode structure having

an electrode including a metal layer 72 and a diffusion barrier layer 74 provides a diffusion barrier preventing diffusion of undesirable materials. A memory device such modified hereinafter is simply referred to as the '247/821/801 reference.

The various materials and labels recited in **claims 12-22, 30-33** for the electrode including the barrier/buffer/adhesion layer, although deficient from the '247/821/801 reference, are known and available to one of ordinary skill in the art, therefore such selecting would have been obvious to one of ordinary skill in the art at the time the invention was made. For example, consult Ignatiev et al. U.S. Patent 6,473,332 (cited in a previous office action) for a list of the suitable materials for the electrodes and barrier/buffer/adhesion layers contains binary nitrides and ternary nitrides.

5. **Claims 38 and 41-42** are rejected under 35 U.S.C. 103(a) as obvious over Hsu et al. U.S. Patent Application Publication 20040235247 (the '247 reference) in view of Hsu et al. U.S. Patent 6,693,821 (the '821 reference) and further in view of Gudesen et al. U.S. Patent Application Publication 20030179617 (the '617 reference), and further in view of Slaughter et al. U.S. Patent 6,544,801 (the '801 reference).

The '247/821/617 reference discloses a memory device as claimed and as detailed above for claims 1, 25, and 33 including a top metal layer that is not a refractory metal, not stable at the high temperature, not stable at the minimum temperature required for fabrication of the memory element, and is not stable at the first temperature, but fails to teach that the bottom electrode further includes another metal layer or conductive metal oxide layer as claimed and that functions as a barrier/buffer/adhesion layer.

However, at the time the invention was made, Slaughter discloses a memory system including a memory cell 50 comprising a bottom electrode structure 54 having an electrode including a metal layer 72 and a barrier/buffer/adhesion layer 74 so as to provide a diffusion barrier preventing diffusion of undesirable materials onto underlying, previously formed layers.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the electrode layer of the '247/821/617 reference such that it includes a barrier layer. One would have been motivated to make such a change because Slaughter teaches that a memory system including a memory cell comprising a bottom electrode structure having an electrode including a metal layer 72 and a diffusion barrier layer 74 provides a diffusion barrier preventing diffusion of undesirable materials. A memory device such modified hereinafter is simply referred to as the '247/821/617/801 reference.

6. **Claim 24** is rejected under 35 U.S.C. 103(a) as obvious over Hsu et al. U.S. Patent Application Publication 20040235247 (the '247 reference) in view of Hsu et al. U.S. Patent 6,693,821 (the '821 reference) and further in view of Johnson et al. U.S. Patent 6,034,882 (cited in a previous office action).

The '247/821 reference discloses a memory device as claimed and as detailed above for claim 1, but fails to teach that that the memory device comprises at least 2 memory arrays, whereby the at least 2 memory arrays are stacked upon one another.

Johnson, in also disclosing a memory device, teaches that a memory device comprises at least 2 memory arrays, whereby the at least 2 memory arrays are stacked upon one another, increases density (Abstract).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '247/821 reference's memory device such that it comprises at least 2 memory arrays, whereby the at least 2 memory arrays are stacked upon one another. One would have been motivated to make such a change because stacked memory device including at least two stacked memory arrays increases density. A memory device such modified hereinafter is simply referred to as the '247/821/882 reference.

7. **Claim 43** is rejected under 35 U.S.C. 103(a) as obvious over Hsu et al. U.S. Patent Application Publication 20040235247 (the '247 reference) in view of Hsu et al. U.S. Patent 6,693,821 (the '821 reference) and further in view of Gudesen et al. U.S. Patent Application Publication 20030179617 (the '617 reference), and further in view of Monsma et al. U.S. Patent 6,331,944 ('the '944 reference).

The '247/821/617 reference discloses a memory device as claimed and as detailed above for claims 1, 25, and 33 including the memory plugs, but fails to teach that each of the memory plugs includes a non-ohmic device as claimed.

However, at the time the invention was made, Monsma teaches, as detailed above in paragraph A.c, that a simple steering device, such as a non-ohmic diode device – rather than a transistor - as a design selection, was fabricated in series with a memory cell so as to obtain a simple structure with only two terminals per cell (Figs. 1-2 and column 3, lines 3-28).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the memory plug such that it includes a non-ohmic device. One would have been motivated to make such a change because Monsma teaches that a memory

system including a memory plug having a non-ohmic diode device forms a simple structure with only two terminals per cell.

8. **Claim 45** is rejected under 35 U.S.C. 103(a) as obvious over Hsu et al. U.S. Patent Application Publication 20040235247 (the '247 reference) in view of Hsu et al. U.S. Patent 6,693,821 (the '821 reference) and further in view of Johnson et al. U.S. Patent 6,034,882 (cited in a previous office action), and further in view of Gudesen et al. U.S. Patent Application Publication 20030179617 (the '617 reference).

The '247/821/882 reference discloses a memory device as claimed and as detailed above for claim 24, comprising at least 2 memory arrays, whereby the at least 2 memory arrays are stacked upon one another, and wherein one of the memory arrays is a topmost array. The '247 reference further disclose that all the all of the metal layers (i.e., electrodes), which includes all of the metal layers the below the topmost memory array, are refractory metal layers, but fails to teach that at least one metal layer above the topmost memory layer is not a refractory metal layer. In other words, the '247/821/882 reference fails to teach that the topmost electrode is of a non- refractory metal layer, or still in other words, fails to teach that the topmost electrode is of a low-processing-temperature material.

However, at the time the invention was made, Gudesen teaches choosing a low-processing-temperature material for the top electrode so as to minimize the diffusion of the top electrode material into the previously formed underlying memory layer.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the top electrode layer of the '247/821/882 reference such that it is a

low-processing-temperature material. One would have been motivated to make such a change because Gudesen teaches choosing a low-processing-temperature material for the top electrode minimizing the diffusion of the top electrode material into the previously formed underlying memory layer.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
June 03, 2005

David Nelms
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